IN THE CLAIMS

1. (Currently Amended) An address input buffer in a semiconductor memory device, comprising:

a differential amplifying means for differentially amplifying a reference voltage and an external address signal; and

a controlling means for ~~controlling the differential amplifying means~~ generating a bias control signal by receiving a refresh signal and a bank active signal to control the differential amplifying means,

wherein activation of the bias control signal depends on the bank active signal when the refresh signal is abnormally activated in an initialization process.

2. (Original) The address input buffer as recited in claim 1, wherein the controlling means further receives a power down signal.

3. (Currently Amended) The address input buffer as recited in claim 2, wherein the controlling means includes:

a NAND gate receiving the refresh signal and the bank active signal;

an inverter receiving an output of the NAND gate; and

a NOR gate receiving an output of the inverter and the power down signal to output the bias control signal.

4. (Currently Amended) An address buffer in a semiconductor memory device, comprising:

a differential input unit receiving a reference voltage and an address signal;

a current mirroring unit connected between the differential input unit and a first voltage;

a biasing unit, which is connected between the differential input unit and a second voltage, for supplying bias current to the differential input unit and the current mirroring unit; and

a controlling unit for ~~enabling/disabling the biasing unit~~ generating a bias control

signal by receiving a refresh signal and a bank active signal to enable/disable the biasing unit, wherein the bias control signal is activated if the refresh signal is abnormally activated in an initialization process.

5. (Original) The address input buffer as recited in claim 4, wherein the controlling unit further receives a power down signal.

6. (Currently Amended) The address input buffer as recited in claim 5, wherein the controlling ~~means~~ unit includes:

a NAND gate receiving the refresh signal and the bank active signal;

an inverter receiving an output of the NAND gate; and

a NOR gate receiving an output of the inverter and the power down signal to output the bias control signal.

7. (Original) The address input buffer as recited in claim 6, wherein the differential input unit, the current mirroring unit and the biasing unit constitutes a differential amplification circuit of a PMOS type.

8. (Currently Amended) The address input buffer as recited in claim 5, wherein the controlling ~~means~~ unit includes:

a NAND gate receiving the refresh signal and the bank active signal;

a first inverter receiving an output of the NAND gate;

a NOR gate receiving an output of the first inverter and the power down signal; and

a second inverter receiving an output of the NOR gate to output the bias control signal.

9. (Original) The address input buffer as recited in claim 8, wherein the differential input unit, the current mirroring unit and the biasing unit constitutes a differential amplification circuit of an NMOS type.

10. (Original) The address input buffer as recited in claim 5, further comprising a CMOS inverter connected to an output node provided in the differential input unit.

11. (Original) The address input buffer as recited in claim 5, further comprising a precharge unit for precharging the output node in response to an output signal of the controlling unit.